ADVANCED FUNCTIONAL MATERIALS

Supporting Information

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High Electric Field Carrier Transport and Power Dissipation in Multilayer Black Phosphorus Field Effect Transistor with Dielectric Engineering

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Supporting Information

S1 (Relationship between breakdown power and channel width)

We fabricated BP devices with different channel widths (W) to ascertain their relationship with the breakdown power (P_{BD}). Towards this end, devices with three different widths, *i.e.* 3.67µm, 5.9µm and 6.75µm were fabricated on the same BP flake, all having ~1 µm channel length (L). As explained in the main text, we conduced study on the electrical breakdown and recorded their P_{BD} as indicated in Figure S1a. Similar to the case of different L, P_{BD} scaled linearly to W and this result convinced that P_{BD} depends linearly on foot-print area ($L \times W$) rather than L or W individually [see Figure S1b].

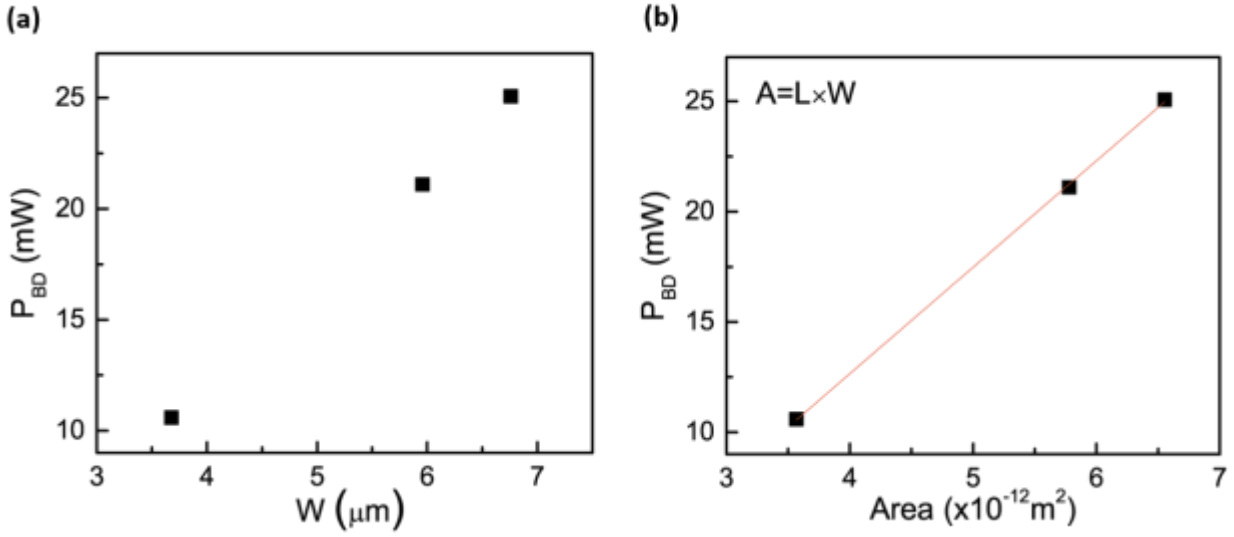

Figure S1. Breakdown power vs. channel width. a) The measured P_{BD} at V_G = 0 from BP devices having same channel length and with three different widths. **b)** P_{BD} plotted agianst foot-print area.

S2 (Extraction of contact resistance)

We extracted contact resistance (R_c) of BP device by using transfer length method (TLM).[1] The low field transfer curves of devices with different L are given in Figure S2a, obtained from BP device shown in the inset of Figure 2c in the main text. All the given BP devices shows dominant p-type behavior, however the longer channel (L_5) exhibits higher hole

current level which increases by reducing L towards shorter channels *i.e.* from L_5 to L_1. Moreover, we extracted the total resistance (R) of all five devices at the higher applied electric field (near breakdown point), and the result showed linear trend to the L as shown in Figure S2b and thereby lineally extrapolating the plot to the y-axis, we obtained R_c of 700 Ω at $V_G = 0$.

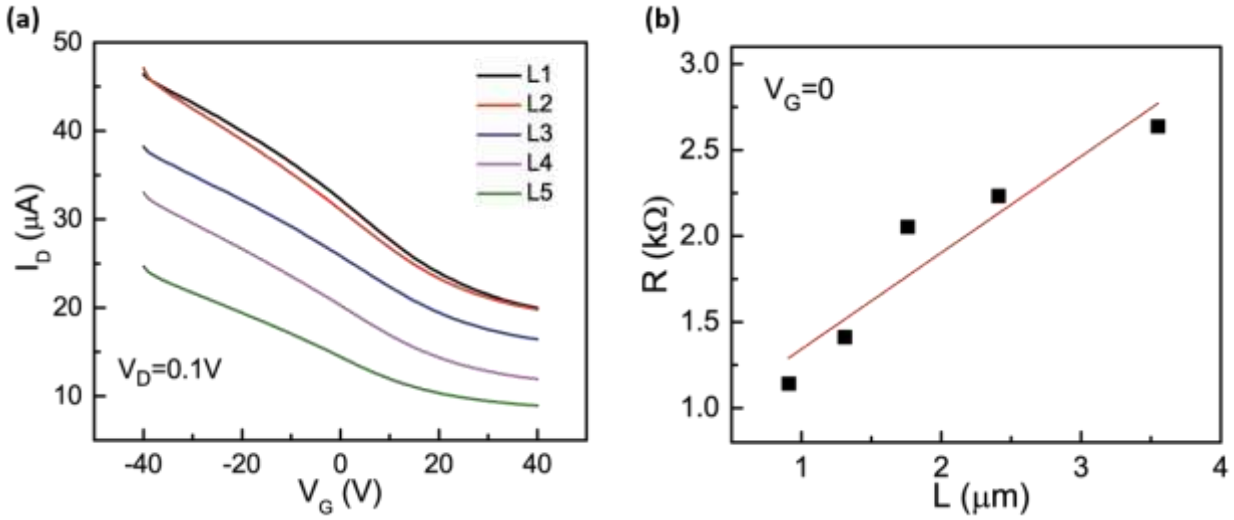

Figure S2. Extraction of contact resistance. a) The transfer curves of BP devices with different L at $V_D = 0.1$ V. **b)** Total resistance of the BP devices at high field condition and $V_G = 0$. The black squares indicate measured data points.

S3 (Interfacial thermal conductance of BP-dielectric interfaces)

We prepared two different kinds of BP-dielectric interfaces, that is, BP-SiO_2 and BP-hBN and deduced their interfacial thermal conductance (G) values. For this, firstly BP devices with six different thicknesses were fabricated on SiO_2 substrate, and their G value ranges from 2 to 10 M W/m^2·K. Thereafter, we fabricated BP devices with two different thicknesses on hBN substrate and similarly using size-dependent analytical model, we computed their G values and the obtained results spanned in the range of 3 to 5 M W/m^2·K. The difference between the values of the two interfaces may be due to different condition of their particular interface and more importantly the different thickness of BP and hBN used. It is important to note that the average G

value of the BP-hBN interface is smaller than that of the BP-SiO_2 interface, and we think this may be due to the thermal healing effect of electrode in the latter case. The breakdown position of BP on SiO_2 substrate was always located in the vicinity of electrodes, as shown in Figure 5 of the main text. In that case, the heat may dominantly sink through electrodes. Therefore, we think the large average G value of BP on SiO_2 can be obtained due to the contribution of metal electrodes. More importantly, this also shows that *G* may not be limited by thermal properties of dielectric itself.

S4 (Calculation of electrical heating coefficients)

The temperature dependent Raman shift can be used to define the vibration properties such as electro-phonon phonon-phonon coupling, or thermal expansion of materials.[2,3] Similarly, based on high field transport induced self-heating coupled with micro-Raman processing, it is possible to extract the electrical heating coefficients of Raman modes of multilayer BP.

For this, we deconvoluted the Stokes mode Raman intensities of multilayer BP on SiO_2 and hBN substrates as a function of applied electric bias from Figure 4a and 4b of the main manuscript, from which we found that all three spectral peak positions *i.e.* A^1g, B_2g and A^2g of multilayer BP supported on SiO_2 and hBN substrates showed a linearly decreasing trend, as depicted in Figure S4a and S4b.

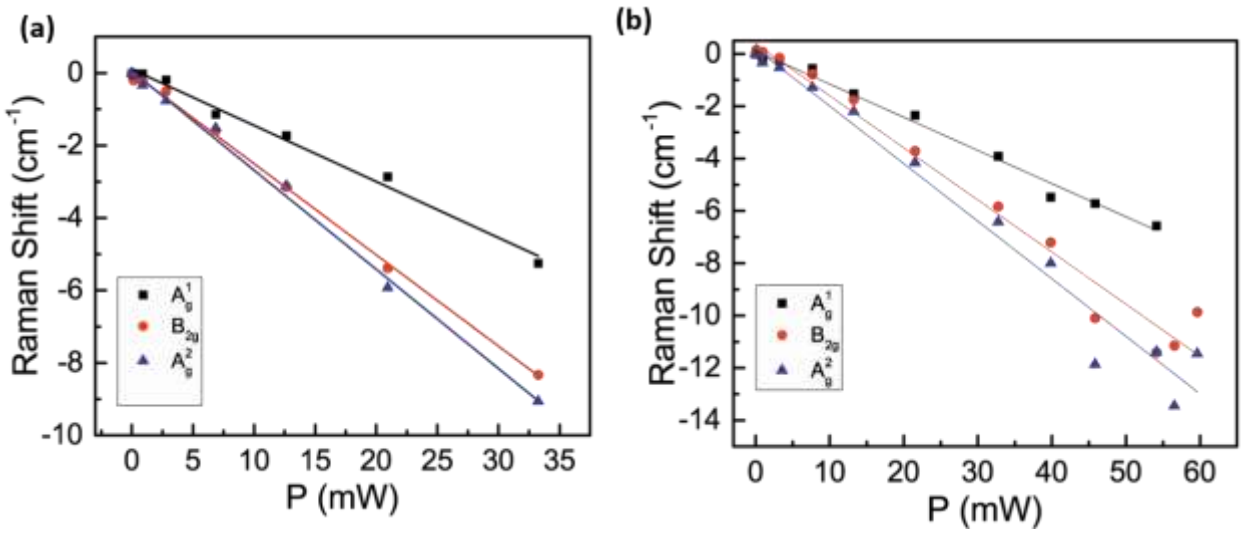

Figure S4. Electrical heating coefficients a) and **b)** The spectral Raman shift of multilayer BP flake as a fucntion of applied electrical power on SiO_2 and hBN substrate respectively. The lines indicate the linear fits to the data points of specific Raman modes.

From that, we obtained the slopes (Δ) of the specific Raman peak by linearly fitting its data to the applied electric power and the results are listed in Table S3.

BP device	Δ (cm^{-1}/mW)			*g* (cm^{-1}/K)		
	A^1g	B_2g	A^2g	A^1g	B_2g	A^2g
On SiO_2 (this work)	0.154±0.005	0.251±0.004	0.273±0.006	0.026	0.043	0.047
On hBN (this work)	0.126±0.003	0.198±0.009	0.219±0.011	0.024	0.038	0.042
On Al_2O_3 (ref. 5)	0.18±0.05	0.44±0.05	0.5±0.05	0.013	0.033	0.038

Table S3. Comparison of slopes (*Δ*) and electrical heating coefficients (*g*) of specific Raman modes of BP on different substrates.

Subsequently, based on the temperature results of Figure 4e in the main manuscript, we scale the Raman shift of each mode to compute the electrical heating coefficients (*g*) for multilayer BP flake on both substrates. The obtained slope and coefficient values, as shown in

Table S4, are very close to the previously reported numbers by electrical heating of multilayer BP on Al_2O_3 substrate,[4] and they are also on the same order of magnitude to the recently reported thermal heating coefficients of multilayer BP.[2,3]

It is noteworthy that the extracted Δ and *g* values of hBN supported BP flake are smaller than those of SiO_2 supported among our results. It is the matter of fact that the peak shift is readily dependent on thermal expansion coefficient (TEC) mismatch of the given materials.[3] Therefore, we think this is due to difference in TEC mismatch between BP-SiO_2 and BP-hBN interfaces, or the large Raman peak shift of BP on SiO_2 substrate may be attributed to the dominant thermal expansion caused by large temperature gradient due to non-homogeneous thermal spreading. However, further studies are needed to address this difference.

S5 (Analytical extraction of temperature distribution at high electric field)

We employed an analytical model based on heat diffusion equation to extract the temperature distribution for BP device near breakdown point.[5] Here, we assume that thermal conductivity of BP is independent of position and temperature of the device and the applied electrical power is homogeneously distributed along the BP flake on SiO_2 and hBN substrates. The heat diffusion equation is,

$$\frac{\mathrm{d}^2T}{\mathrm{d}x^2}+\frac{1}{\kappa t}\left[\frac{P}{LW}-2G(T-T_{\mathrm{o}})\right]=0, \qquad \text{(S1)}$$

Here, *x* is position along the channel. Now, solving S1 to extract maximum operating temperature as a function of location along the channel *i.e. T(x)* will yield,

$$T(x)=T_{\mathrm{o}}+\frac{P}{c^2\kappa LWt}\left(1-\frac{\cosh(cx)}{\cosh(cL/2)}\right), \qquad \text{(S2)}$$

where $c = \sqrt{2G/kt}$. By applying corresponding values and breakdown power values of 33.25 mW and 59.63 mW for BP on SiO_2 and hBN respectively, we can extract the temperature distribution at breakdown point along the BP devices. It should be noted that our calculated *G* values for BP on SiO_2 and hBN substrates span from 2 to 10 M W/m^2·K and 3 to 5 M W/m^2·K respectively: see Supporting Information S3. However, in this case the best temperature results that were in agreement with experimentally calculated values, were obtained at *G* values of 3 M W/m^2·K and 5.1 M W/m^2·K for BP-SiO_2 and BP-hBN interfaces respectively, as shown in Figure S5a and S5b.

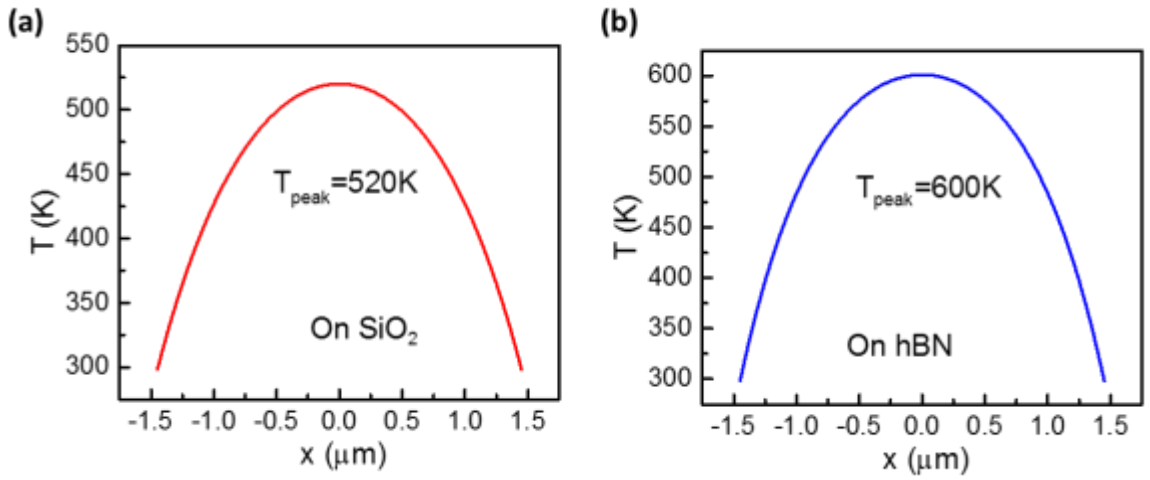

Figure S5. Temperature distribution at high electric field a) and **b)** The obtained temperature profiles of SiO_2 and hBN supported BP deviecs, with peak temperatures of 520 K and 600 K respectively.

Nonetheless, at all the given *G* values, the obtained temperature profiles were similar *i.e.* dome shaped plot while they differ in peak temperature values. Furthermore this profile indicates that, the center is heated, while contacts remain at room temperature. The readers may argue over the peak temperature position on SiO_2 substrate, since the hotspot location was near to the electrode from the optical microsope image [see Figure 5b in the main manuscript]. This

contradiction is due to the fact that, in given model, we assume uniform power distribution. This model is more realistic for hBN supported or suspended devices since charge trapping at the dielectric is minimum or absent, which enables uniform power distribution along the BP device.

S6 (Analytical calculation of operating device temperature as a function of applied electrical power)

Next, we also computed operating temperature as a function of applied power by modifying equation S2. Since the operating temperature is maximum at the center of the flake, therefore setting $x = 0$ in S2,

$$T(P) = T_o + \frac{P}{c^2 \kappa LWt}\left(1 - \frac{1}{\cosh(cL/2)}\right), \qquad \text{(S3)}$$

Similarly, using G values of 3 M W/m^2·K and 5.1 M W/m^2·K for BP-SiO_2 and BP-hBN interfaces respectively, we extracted temperature as a function of applied power for both the cases, as shown by solid line in Figure 4e of the main manuscript. The computed results coincide well with experimentally calculated temperature values.

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